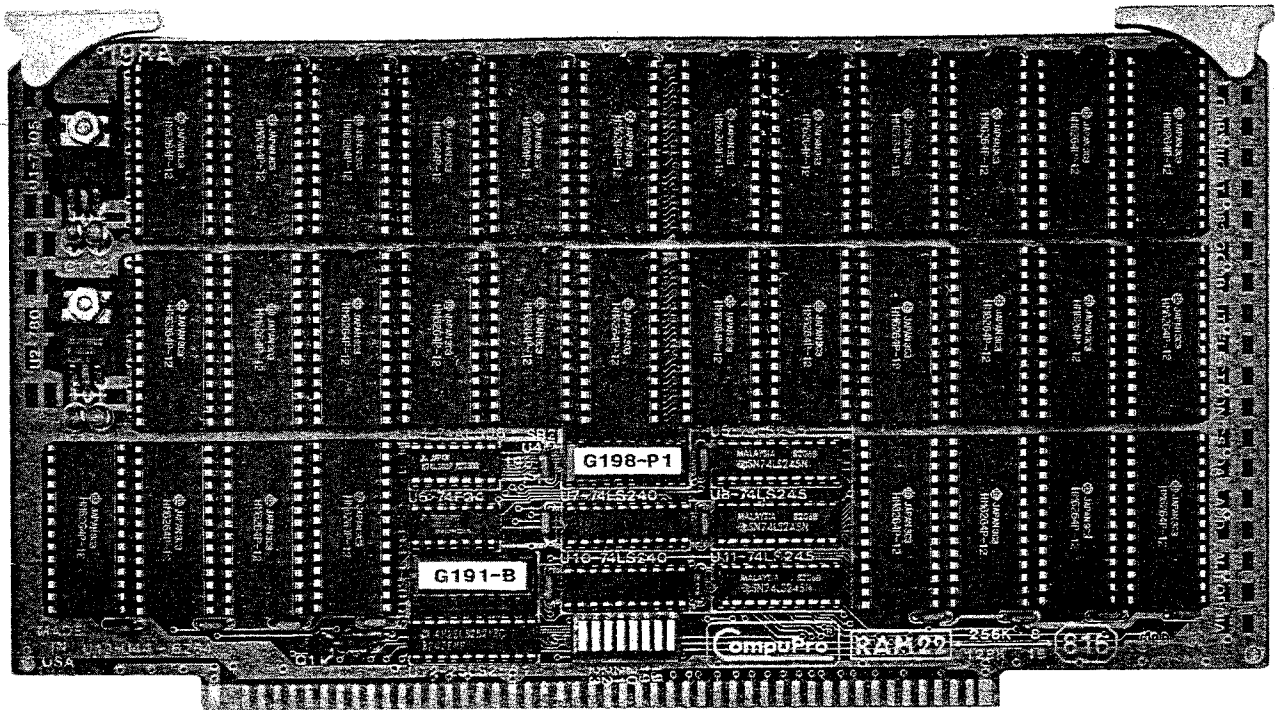


RAM 22™

TECHNICAL MANUAL



IEEE 696 / S-100

STATIC MEMORY

256K x 8 or 128K x 16

198A

mac



CompuPro.

a Godbout Company

3339 Arden Road
Hayward, CA 94545

(415) 786-0909

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NEW
ADDRESS

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RAM 22 TECHNICAL MANUAL

ABOUT RAM 22

The RAM 22 from **CompuPro** represents one of the most advanced RAM boards ever produced for the IEEE 696/S-100 Bus. Combining state-of-the-art static CMOS RAM technology with **CompuPro's** design excellence makes the RAM 22 the most versatile, efficient and reliable RAM available today. The RAM 22 works as a "byte-wide" memory in 8 bit systems and automatically switches to "word-wide" mode for today's newer 16 bit systems. The RAM 22 is the choice of professionals for scientific, industrial and commercial applications where the emphasis is on full speed operation with the advanced CPUs of today and tomorrow while maintaining downward compatibility with 8 bit CPUs.

TECHNICAL OVERVIEW

The RAM 22 uses thirty-two high performance 8K X 8 CMOS RAM chips to provide a total of 256K bytes or 128K words of storage. The RAM 22 is addressable on any 256K byte boundary in the 16 megabyte address space specified by the IEEE 696 standard.

The RAM 22 also dynamically switches between "byte-wide" or "word-wide" modes per the state of the sXTRQ* signal on the S-100 Bus (see the Theory of Operation section for a complete discussion of how this protocol works).

The RAM 22 was designed to work with 8086/88 type processors at speeds exceeding 10 MHz. It also handles DMA flawlessly, a feature few boards can boast.

To reduce the number of support ICs required to pack all this function and capacity onto a standard height S-100 board, two PAL (programmable-array-logic) elements are used. The PAL selects the proper memory chips and controls the complicated data bus switching scheme required to mix 8 and 16 bit operations.

All of this goes onto a high-quality double-sided circuit board that has a full solder-mask and legend. Sockets are provided for all ICs for ease of maintenance. All edge connector contacts are gold on a nickel substrate to insure long and reliable operation.

NOTE: This board does not allow any of the four 64K blocks on the board to be disabled.

HOW TO CONFIGURE THE RAM 22 FOR YOUR SYSTEM

The RAM 22 requires only that the starting address of the board be set using switch S1. All other features such as PHANTOM and byte (8 bit)/word (16 bit) transfers are handled automatically by onboard logic. This board responds to the upper eight address lines (A16-23) as provided for by the IEEE 696/S-100 standard.

The starting address of the board is selected by setting the middle six paddles of dip-switch S1. S1 is located near the bottom center of the board. The address is set in a binary fashion with each paddle of S1 representing an address bit. An "ON" paddle represents a binary "zero" and an "OFF" paddle represents a binary "one". The paddle to address bit relationship is shown in the following table:

SWITCH SETTINGS FOR S1 - ADDRESS SELECTION

ADDRESS BIT	PADDLE NUMBER	
A23	2	
A22	3	
A21	4	ON = 0
A20	5	OFF = 1
A19	6	1&8 = not connected
A18	7	

EXAMPLE: If this is the first RAM board in your system and you want 256K starting at address 000000H, set paddles 2 through 7 of S1 ON.

EXAMPLE: If this is the second 256K board in the above system and you want it addressed at 040000H set paddles 2 through 6 ON and paddle 7 OFF.

EXAMPLE: If you want this board to reside at the top of the first megabyte of address space (i.e., starting address 0C0000H), set paddles 2 through 5 ON and paddles 6 and 7 OFF. Incidentally, this would put the board at the highest 256K address which an 8086 or an 8088 can directly address.

THEORY OF OPERATION

The RAM 22 is designed to work in 8 and 16 bit systems per the protocol established by the IEEE 696/S-100 standard. The DATA IN and DATA OUT buses operate as a bidirectional 16 bit data path when word transfers are performed. The two buses remain unidirectional during byte operations.

Here's how the protocol works: The bus master requests a 16 bit transfer by asserting sXTRQ* (line 58 low). If the slave (in

this case the RAM 22) is capable of performing word transfers, it acknowledges this fact to the master by asserting SIXTN* (line 60 low). Sometimes, even a 16 bit master may only want to transfer one byte rather than a whole word. In this case, the master does not assert sXTRQ* but instead uses the data buses as an 8 bit master would, that is: data from the master would be transferred on the D0 bus and data to the master would be transferred on the D1 bus.

The RAM 22 handles this multiplexing of the data buses with two bidirectional bus buffers (U5 and U11) and one intermediate buffer (U8) Both U5 and U11 are enabled for all word transfers. Both U5 and U11 are enabled for word read operations. When byte writes occur with A0=0, U15 is enabled. When byte writes occur with A0=1, U5 and U8 are enabled. When byte reads occur with A0=0, U8 and U11 are enabled. When byte reads occur with A0=1, U11 is enabled.

This complicated algorithm is executed by PAL (programmable array logic) element G191 (U9). A second PAL (U4) acts as the array decoder along with U3. The RAM is configured as two arrays of 128K by 8 bits, A and B. The bit/address decode scheme is covered in the next section. The decoder PAL only generates select signals, which enable the RAM chips only during memory reference operations. This feature, coupled with the use of RAM chips which power down when not selected makes the RAM 22 consume less power than most dynamic RAM designs while providing the speed of operation and reliability that only static RAM delivers.

The base address of the board is set with dip-switch S1. Octal comparator (U8) generates signal BSEL* when the address present on bus lines A18 through A23 matches that set in S1-2 through S1-7. Positions 1 and 8 of S1 are not used.

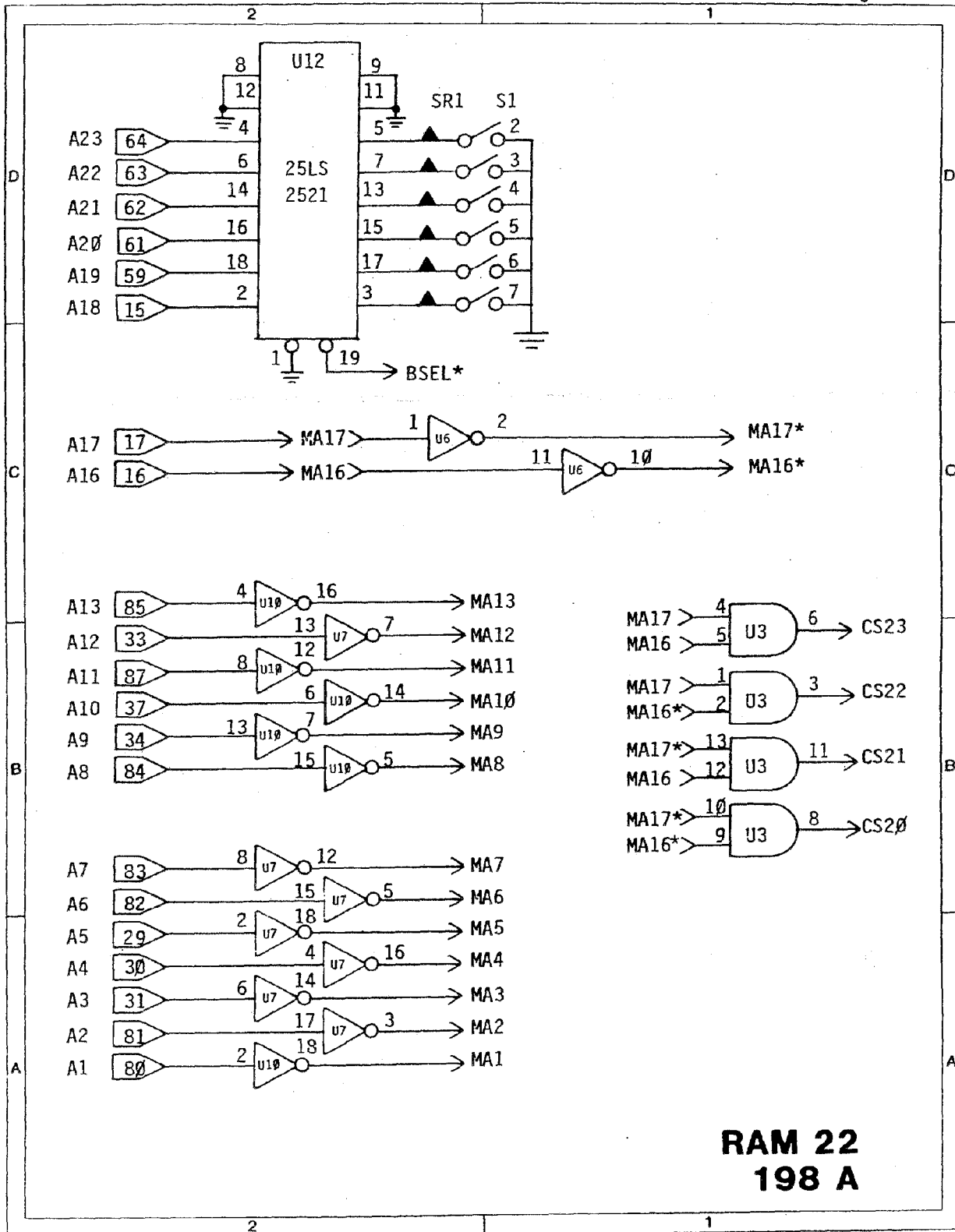
ESXT* is the signal generated in the PAL (U9) which causes the RAM 22 to acknowledge requests for word transfers when the board is selected. Transistor Q1 provides the open collector output required to drive bus signal SXTN* (line 60).

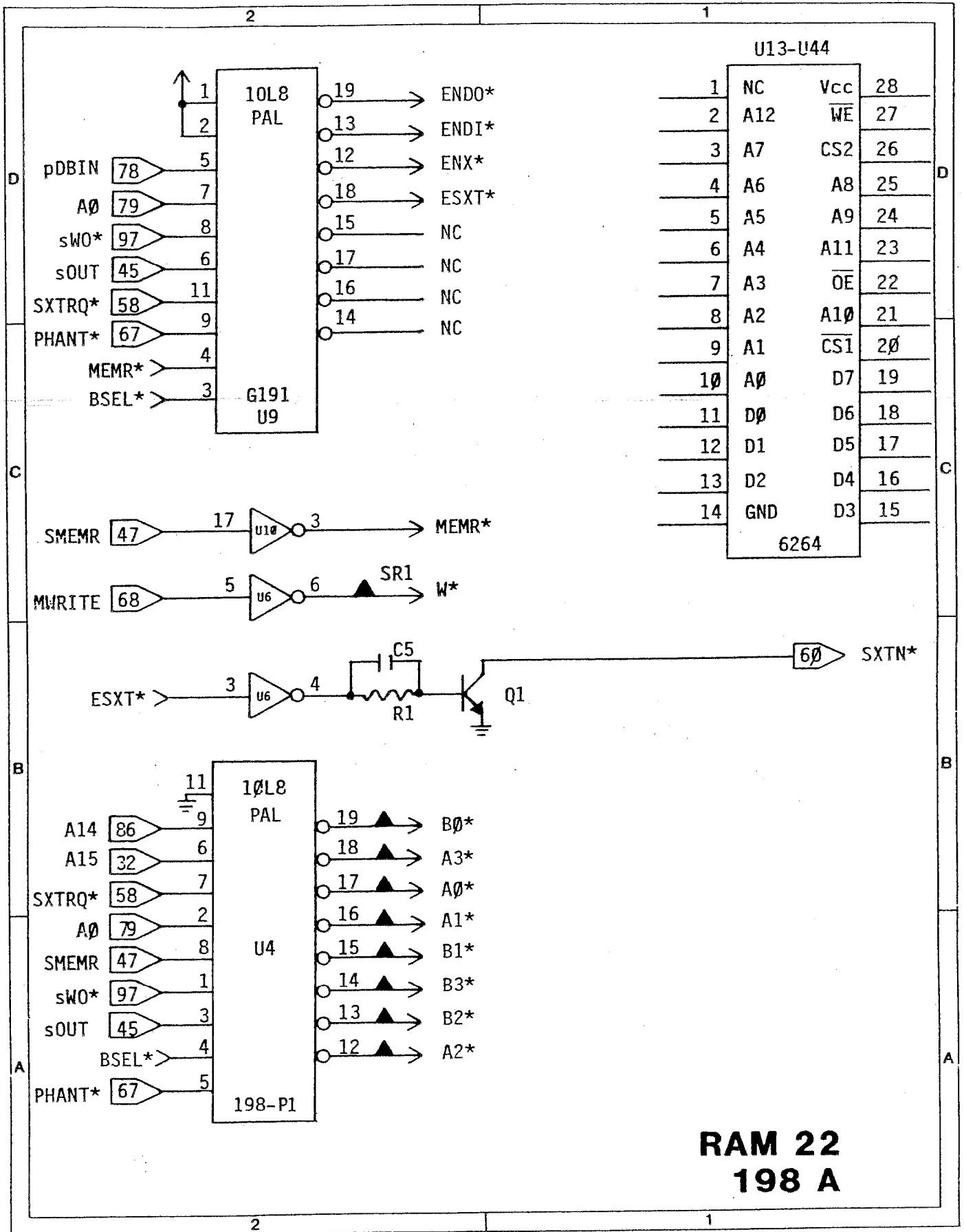
LOCATING RAM ICs BY ADDRESS AND BYTE

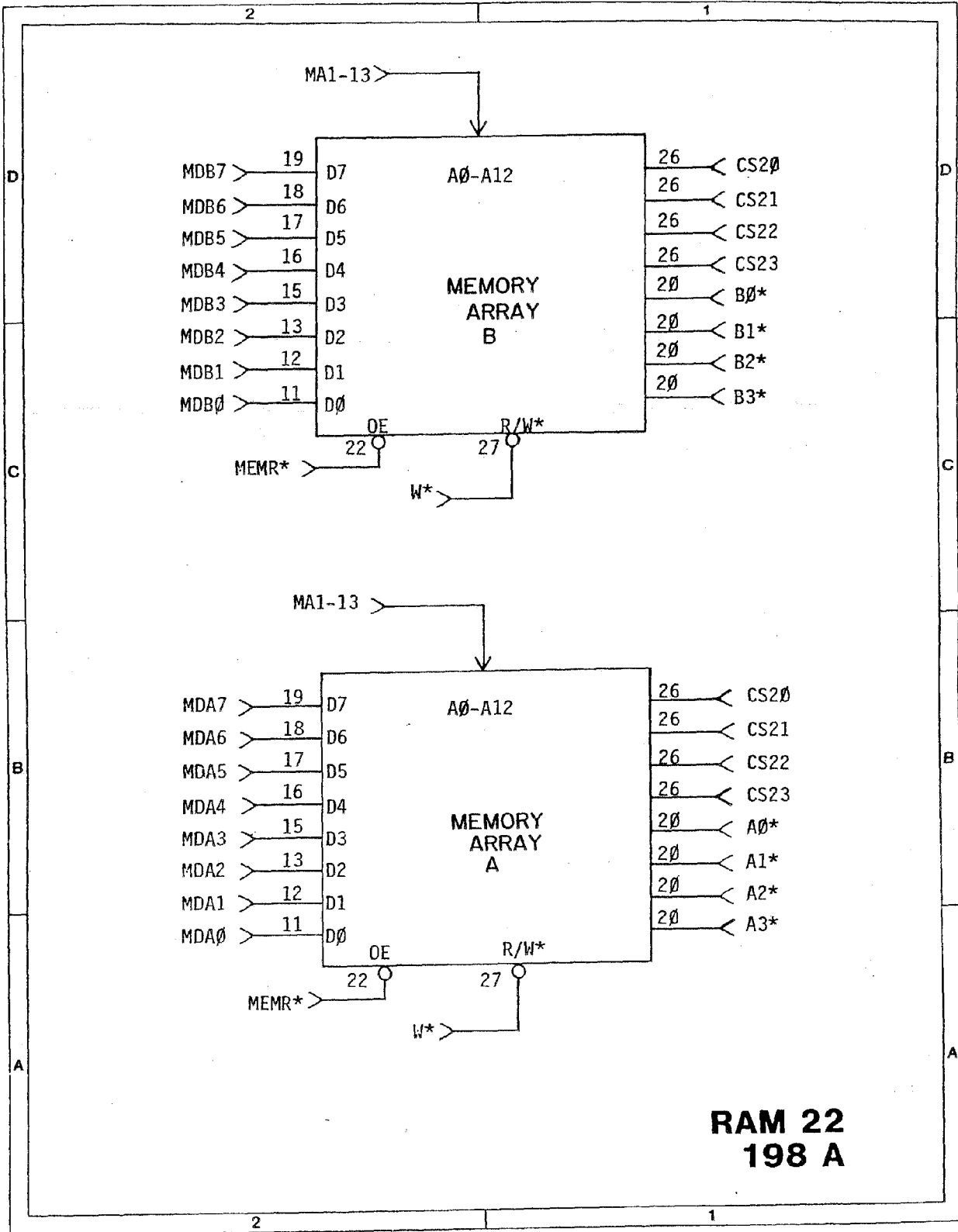
The COMPONENT LAYOUT at the back of this manual may be used as a map to locate RAM ICs by address and byte. Each RAM chip is identified by address and high or low byte position.

In the byte or 8 bit mode only one RAM is selected. All even bytes, A0 in the zero state, are in array A. All odd bytes, A0 in the one state, are in array B.

In the word or 16 bit mode, two RAM chips are enabled. One RAM chip in the odd array and one RAM chip in the even array.







PARTS LIST

SEMICONDUCTORS

Q1	MPS 3646
U1,2	7805
U3	74ALS08
U4	G198-P1
U5,8,11	74LS245
U6	74ALS04
U7,10	74LS240
U9	G191
U12	25LS2521
U13-44	HM6264

CAPACITORS

C1-4	10V/higher dipped tantalum
C5	68 pF dipped mica
(26)	bypass capacitors

RESISTORS

R1	1.5K Ohm
SR1,2	5.1K Ohm SIP - 10 pin

MISCELLANEOUS

S1	8 position DIP switch
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**COMPUPRO
RECEIVING/SERVICE CENTER—REPAIRS
3339 ARDEN ROAD
HAYWARD, CA 94545**

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CompuPro will repair or replace, at our option, any parts found to be defective in either materials or workmanship for a period of 1 year from date of invoice. Defective parts **MUST** be returned for replacement.

If a defective part causes a CompuPro product to operate improperly during the 1 year warranty period, we will service it free (original owner only) if delivered and shipped at owner's expense to and from our **Service Center at 3339 Arden Road, Hayward, CA 94545**. If improper operation is due to error or errors on the part of the purchaser, there may be a repair charge. Purchaser will be notified if this charge exceeds \$75.00. If the warranty period has expired, service for CompuPro products is available at a labor rate of \$50.00 per hour plus parts.

We are not responsible for damage caused by use of solder intended for purposes other than electronic equipment construction, failure to follow printed instructions, misuse or abuse, unauthorized modifications, use of our products in applications other than those intended by CompuPro, theft, fire, or accidents.

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